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S/N09/431477 PATENT

Atty
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicant: | Kiran Ganesh et al. | Examiner: | Phallaka Kik |
| Serial No.: | 09/431477 | Group Art Unit: | 2825 |
| Filed: | November 1, 1999 | Docket No: | 884.141US1 |
| Title: | 2-DIMENSIONAL PLACEMENT WITH RELIABILITY CONSTRAINTS FOR VLSI DESIGN | | |
| Customer No.: | 21186 | Assignee: | Intel Corporation |

**AMENDMENT UNDER 37 C.F.R. §1.116**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please amend the above-identified patent application as follows.

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